A 4K2K 60-fps Image Sensor Based on Stagger-laced Dual-exposure Technique

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***Abstract*—This study describes a 12-bit, 4K2K 60-fps CMOS image sensor capable of reducing the pixel readout rate without degrading resolution of the output images. The data reduction is done by a novel "stagger-laced" scan, which reduces the data rate by half by alternate readout of two sets of horizontal pixel pairs arranged in two complementary checkerboard patterns. For the 12-bit, 60-fps readout of 4K2K pixels, the column delta-sigma (ΔΣ) ADCs are employed. The chip is fabricated using imec 130-nm 1P3M CMOS process. Experimental results show the proposed stagger-laced scanning followed by an image restoration process little degrades the image resolution from the progressive one in spite of the half number of pixels read out, as well as enhances the image SNR.**

I. INTRODUCTION

Recently, the increase of the number of pixels on image sensors knows no boundaries in both video and still camera uses. In addition, requirements for the frame rate and the bit resolution of the images are also growing higher. Under these circumstances, there are growing demands for the high-speed imaging, and several approaches for high-speed imaging including new ADC topologies have been researched and presented: e.g. single-slope ADCs with high-speed clocks [1], successive approximation ADCs [2], delta-sigma (ΔΣ) ADCs [3] and cyclic ADCs [4].

On the other hand, high-speed imaging has another problem: extremely high data output rate. This may impose a large burden to the data receivers in camera sets, resulting in increase of the power consumption as well as the size of camera systems, which are prominent matters especially for consumer-use digital cameras. For digital video cameras, the interlaced scanning is known as a data reduction approach which can reduce the readout rate by half [5], and is widely used in CCD imagers [6–7] as well as CMOS image sensors [8]. However, the spatial resolution of the interlaced images is somewhat degraded because each frame contains only odd or even line addresses.

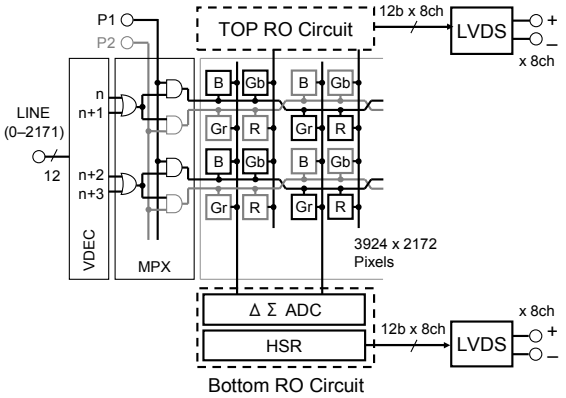

Fig. 1 Block diagram of the 4K2K image sensor.

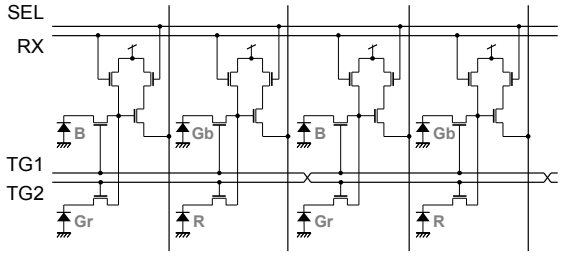

Fig. 2 Pixel circuit.

In this paper, we propose a 4K2K, 60-fps image sensor which achieves high spatiotemporal resolution with a pixel readout rate of a half of the progressive scan. In order to achieve 12-bit A/D-conversion for 4K2K pixels at 60-fps, the column ΔΣ ADCs are employed. For the reduction of the readout rate with keeping the imaging resolution, an imaging framework of a novel "stagger-laced" scanning combined with an image restoration processing is proposed and examined. In addition, performances of the proposed imaging method against the imaging noises are also discussed.

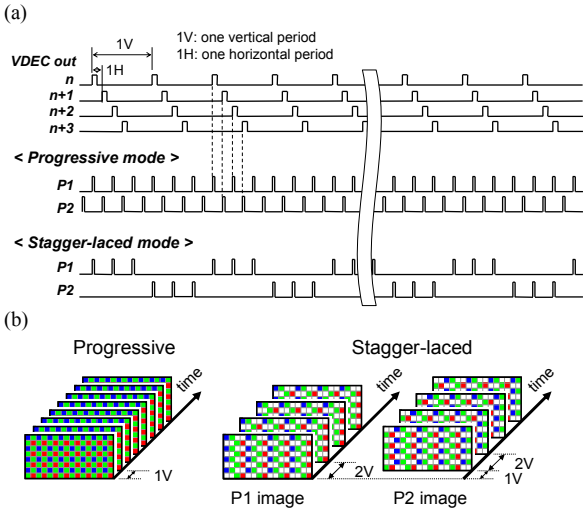

Fig. 3 (a) Pulse timing of the progressive and stagger-laced scan. (b) The resulting images.

II. Device Architecture

The chip architecture is illustrated in Fig. 1. The 4K2K pixels are arranged in a Bayer pattern. The floating diffusion (FD) nodes of 2 vertically adjacent pixel cells are shared, as shown in Fig. 2. The readout circuits composed of column ΔΣ ADCs and horizontal shift registers (HSR) are placed both above and below the pixel array. The HSR outputs are transported out of the chip by LVDS. The vertical decoder (VDEC) drives each horizontal line according to the LINE input. The chip has two different pixel readout pulses, P1 and P2, and the multiplexer (MPX) applies P1 and P2 to TG1 and TG2 signal lines shown in Fig. 2, respectively. On the pixel array, pixel pairs connected to TG1 and pairs connected to TG2 are alternately arranged on each row, enabling pixels connected to TG1 and TG2 can be driven at different timings by supplying P1 and P2 at different timings from each other.

III. Stagger-laced Dual-exposure Scan

A. Timing Scheme

The "stagger-laced" scanning is realized by the mutually time-shifted dual exposure of pixels connected to TG1 and TG2, which receive the readout pulses P1 and P2, respectively. The timing sequence and the resulting images of the stagger-laced scanning are shown in Fig. 3. As shown in Fig. 3 (a), P1 and P2 are output alternately at every two vertical periods for the stagger-laced mode, whereas both P1 and P2 are supplied at every vertical period for the progressive scan mode. During the stagger-laced mode, the output pixel signals of each vertical period are only from what are connected to either TG1 or TG2 signal lines. The resulting captured images become like Fig. 3 (b), in which the number of pixels read out is equal to a half of the progressive scan in each vertical period.

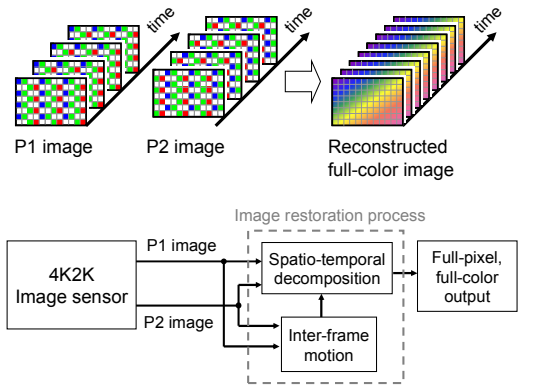

Fig. 4 Image restoration process.

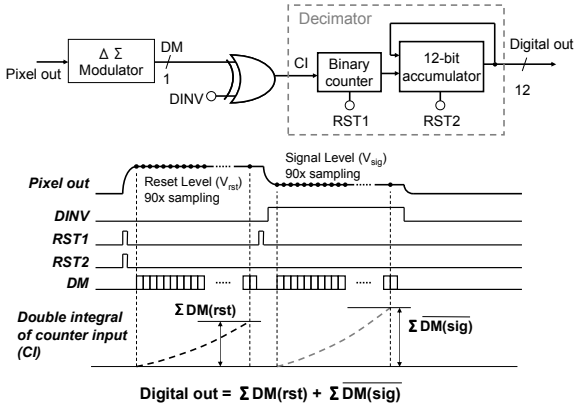

Fig. 5 Block diagram of delta-sigma ADC and its timings.

B. Restoration of the Stagger-laced Images

The pixel signals not scanned in each stagger-laced image are reconstructed by the off-chip image restoration processing [9], and then each stagger-laced image is up-converted to a full-color and full-pixel image. Figure 4 summarizes the image restoration process. The process consists of 2 step blocks: (1) the motion vector detection between the successive P1 and P2 fields, and (2) the spatiotemporal decomposition to reproduce unscanned pixel signals in each P1 and P2 image with utilizing the preliminarily detected motion information.

IV. Column ADC

This image sensor employs the column delta-sigma (ΔΣ) ADCs for realizing 12-bit A/D conversion for 4K2K pixels at 60-fps progressive imaging. The block diagram of the ΔΣ ADC and its timings are illustrated in Fig. 5. The ΔΣ ADC is composed of a 2nd-order ΔΣ modulator and a decimator. The modulator has a feedforward architecture for improved overall linearity despite low-gain amplifiers, and uses auto-zeroed half-delay integrators. The A/D conversion is done twice in one horizontal scan, for the pixel reset and signal levels. The correlated double sampling (CDS) is done digitally by inverting the modulator output during the conversion of the pixel signal level. This architecture allows for

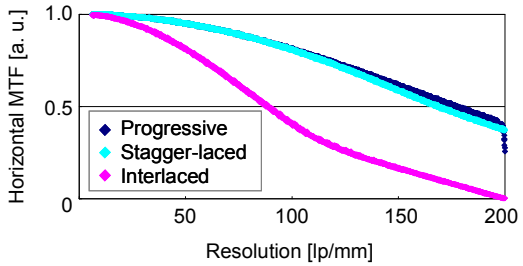

Fig. 6 Measured MTFs of the progressive image, the interlaced image from a complementary-color-filtered imager and the reproduced image from the stagger-laced scanning of the proposed imager.

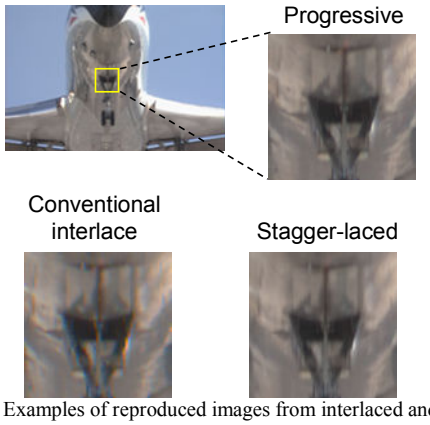

Fig. 7 Examples of reproduced images from interlaced and stagger-laced inputs.

reducing the number of logic inverters involved in the CDS operation by 1/12 (= 1 / (# of bits)) compared to the bitwise inversion [3], achieving reduction of the ADC circuitry.

V. Performance Evaluation

The image reproducibility of the stager-laced scanning is examined by measuring resolution of the output images with respect to the modulation transfer function (MTF). Figure 6 shows the MTFs of the progressive image and the reproduced image by our method. The progressive image is reproduced by de-mosaicing [10] from a Bayer pattern. The plots of MTFs shown in Fig. 6 indicate MTF of the image from the proposed imaging scheme is little degraded from the progressive image. This high resolution is achieved by the image restoration utilizing the spatial correlatedness of pixel signals and the inter-frame motion of the objects, and this stagger-laced pixel arrangement is suitable for this processing. Figure 7 shows sample images of progressive and reproduced from the stagger-laced scan, in which an airplane is moving upward in the image for landing. As shown in Fig. 7, the proposed stagger-laced imaging can achieve comparable resolution with progressive one, in contrast to the reproduced image from conventional interlaced scan in which some degradation in resolution can be perceived.

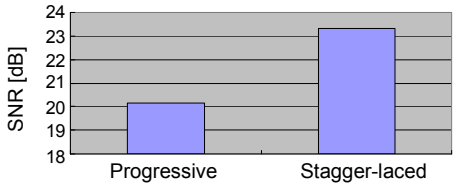

Fig. 8 Measured SNRs of the progressive image and the reproduced image from the stagger-laced scan taken from a noisy scene.

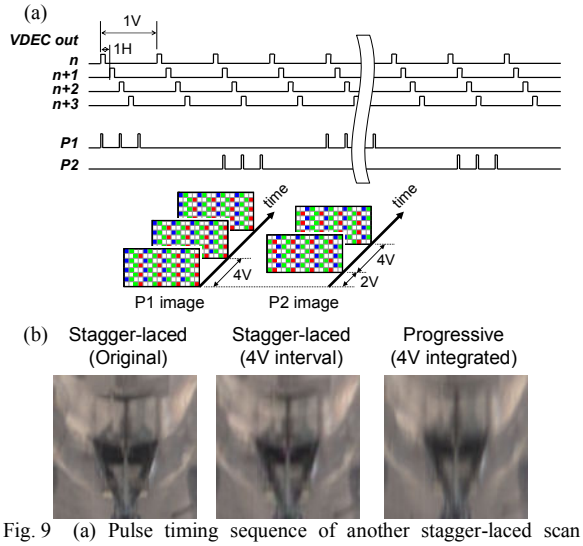

Fig. 9 (a) Pulse timing sequence of another stagger-laced scan pattern with the scan interval of 4 vertical periods and the resulting images. (b) Sample reproduced images from the original and 4V-interval stagger-laced scans and a progressive image with an integration time of 4 vertical periods.

In addition, as shown in Fig. 8, the stagger-laced scanning improved image SNR by 3 dB from the progressive image. This is because the pixel integration time of the P1 and P2 images is extended by twice the progressive scan. The extent of this sensitivity enhancement can be controlled by simply adjusting the pixel integration time, namely the scan interval of the P1 and P2 images. Also, the longer scan interval leads higher compression ratio of the readout rate. Figure 9 (a) shows an example of a driving pattern with a longer scan interval, in which each stagger-laced image is read out at every 4 vertical periods. The measured SNR of the reproduced image from this driving pattern is 25.0 dB, further improved from the "original" stagger-laced scanning. Though motion blurs included in the output image is somewhat increased from the original stagger-laced scan, it is still improved from the progressive image simply integrated for 4 vertical periods (Fig. 9 (b)). Therefore, this imager can be used for both high-resolution imaging with compressed readout rate and high-sensitivity (plus higher compression rate) imaging, whose performances can be controlled by adjusting the scan interval. Here, even in the stagger-laced scan with longer scan interval, resolution of the output images is

TABLE I. CHIP CHARACTERISTICS

Process Technology	imec 130 nm 1P3M
Number of pixels	3924 (H) × 2172 (V)
Number of effective pixels	3840 (H) × 2160 (V)
Pixel size	2.5 um × 2.5 um
Image format	2/3 inch
Scanning	Progressive / Stagger-lace
Frame rate / # of bits	60 fps / 12 bit
Output I/F	12bit-serial LVDS
Output bit rate	5.97 Gbps (Progressive) 2.99 Gbps (Stagger-lace)
Conversion gain	70 uV/ele
Full well capacity	10000 ele
Supply voltage	3.3 V / 2.5 V / 1.2 V
Package	304pin LGA

still better than the simply long-exposed progressive images.

VI. DEVICE CHARACTERISTICS

The main characteristics of the chip are summarized in Table I. The chip is fabricated in imec 130 nm 1P3M process with MIM capacitors and pinned photodiodes. The vertically FD-shared 4T pixels have achieved full-well capacity of 10000 e^-. The pixel pitch is 2.5 μm and the column circuits' pitch is 5 μm. The ΔΣ ADCs are driven by 66-MHz clocks and achieve 12-bit A/D conversion in 1.37 μs. The output bit-rate becomes 5.97 Gbps using the progressive mode, whereas it is reduced to 2.99 Gbps using the stagger-laced mode. Figure 10 shows a top-view photograph of the chip designed and fabricated in this study, and Fig. 11 shows a sample image taken by this imager.

VII. CONCLUSION

In this study, a 4K2K 60-fps image sensor capable of reducing pixel readout rate by half without degradation in resolution based on the stagger-laced scanning is proposed and demonstrated. The 12-bit A/D conversion for 4K2K 60-fps imaging is successfully demonstrated by the column ΔΣ ADCs. The experimental results show the stagger-laced imaging achieves comparable resolution with the progressive images in spite of the half readout rate. This indicates the proposed imager potentially realizes 4K2K 120-fps imaging with the same resolution and readout rate as 60-fps progressive imaging. In addition, a noise reduction performance of the proposed stagger-laced imaging is also demonstrated. By adjusting the scan interval in the stagger-laced scan, this imager is applicable for (1) high-resolution imaging with a half readout rate and/or (2) high-sensitivity and highly data-compressed imaging depending on the applications.

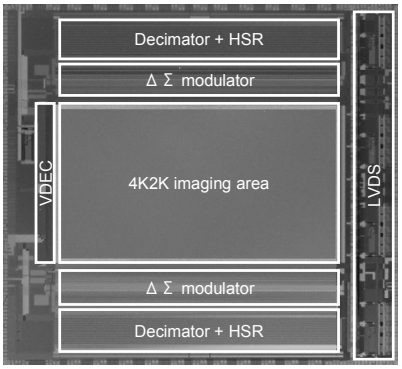

Fig. 10 Chip photograph.

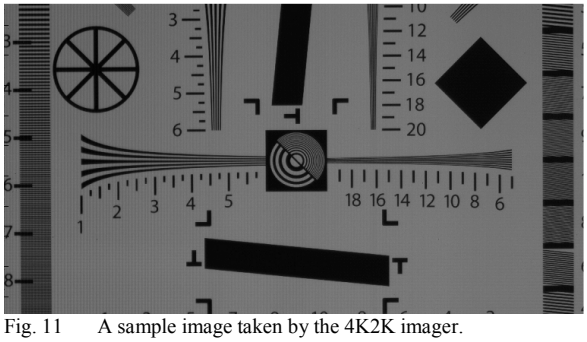

Fig. 11 A sample image taken by the 4K2K imager.

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